3. The disclosure was objected to because the title contained the informality "REFERENCEVOLTAGE". The title has been amended by this paper to contain "REFERENCE VOLTAGE".

4. Claims 14-17 were objected to because of certain informalities. This paper amends claims 14-17 to incorporate the Examiners requested changes.

5. Claims 16-18 were rejected under 35 U.S.C. §112 because the specification does not reasonably provide enablement for every conceivable means of achieving the stated purpose. Claims 16-18 have been amended so they are no longer in single means claim form.

6. Claims 1-3 and 14 and 15 were rejected under 25 U.S.C. §112 as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In particular, these claims were rejected for being incomplete for omitting essential steps, such omission amounting to a gap between the steps. Applicant respectfully traverses.

Claim 1 was rejected because the claimed function/result does not result simply from a single recited step. More particularly, claim 1 was rejected for failing to have the steps of comparing, performing the moving using a counter and a multiplexer, and converting to a digital stage. Claims 2 and 3 were rejected for the same reason noted in claim 1. Claims 14 and 15 were rejected for reasons similar to claim 1.

Claim 1 has been amended to state the limitation "wherein said reference voltage is compared to said received voltage level to determine a digital state..." as a step. Although this change results in a claim that is no less broad, applicant believes that it is clearer to state this limitation as a separate step since it will typically (but not necessarily) be performed by different hardware than the step of moving.

Applicant respectfully disagrees with the Examiner's position that the recited steps need to be added to claims 1-3 and 14-15 to meet the definiteness requirements

of 35 U.S.C. §112 and applicant also respectfully submits that the Examiner has not established a *prima facie* case for indefiniteness. The section of the MPEP cited by the Examiner in support of this rejection states: "a claim which fails to interrelate essential elements of the invention *as defined by applicant(s) in the specification* may be rejected...for failure to point out and distinctly claim the invention." (emphasis added) MPEP 2172.01. Applicant respectfully submits that applicant's specification does not define *as essential* any of the elements recited by the Examiner (i.e. performing the moving using a counter and a multiplexer, etc.) as essential elements. Therefore, without further explanation or to particularly point out where and with what language applicant has defined these elements as *essential* in *applicant's specification* (or other correspondence on the record), applicant respectfully submits that a *prima facie* case for indefiniteness has not been established by the Examiner.

In addition, applicant would like to point out that before a typical electronic device can function, it must first be supplied with power before it will function. Therefore, a step of supplying power may be seen as an essential element to any method claim that involves and electronic device. However, courts have upheld as valid many claims involving electronic devices without such a step. Accordingly, not every element or step disclosed in applicant's specification is necessary or essential and therefore must be placed in a claim to meet §112's requirements for definiteness.

7. Claims 1, 4-6, 8, 10, and 12-21 were rejected under 35 U.S.C. §102(b) as being anticipated by Lippmann et al. (U.S. Pat. #5,233,329). Applicant respectfully traverses. Lippmann discloses a system that *increases* the difference between the reference voltage level and the received voltage level. This process is described in column 5, lines 15-39. For this discussion, note that the reference signal at tap **18** is shown in figure 1 to be connected to a tap in the resistor ladder that closer to V_{IGN} than the reference voltage at tap **18** Therefore, the voltage at tap **18** is greater than the voltage at tap **22**. Starting at column 5, line 15 of Lippmann:

"When the signal data from sender **38** is of sufficient level....the control signal [36] goes high. The high logic level on line **36**, toggles multiplexer **28** so that the lower reference voltage at tap **22** is coupled to line **31**...."

In other words, when the signal voltage level of Lippmann is *above* the reference voltage, the control signal goes high toggling the multiplexer to *reduce* the reference voltage. Since the signal voltage is already *above* the reference voltage, *reducing* the reference voltage *increases* the difference between the reference voltage and the received voltage level.

Likewise, starting at column 5, line 30 of Lippmann:

"When the signal ... is lower than the reference ... the comparator output **30** is low, selecting up/down counter **32** to count down with every clock.... When up/down counter **32** underflows... the control signal on line **36** [goes] low. When the control signal on line **36** goes low, the inverting input of comparator **30** is again coupled to the first reference signal at tap **18**...."

Accordingly, when the signal voltage level of Lippmann is *below* the reference voltage, the control signal goes low toggling the multiplexer to *increase* the reference voltage. Since the signal voltage is already *below* the reference voltage, *increasing* the reference voltage *increases* the difference between the reference voltage and the received voltage level.

Applicant's claim 1 calls for a <u>second voltage level that is closer to a received voltage level....</u> Claims 4 and 6 call for <u>adjusting...to reduce a difference....</u> Claim 8 calls for <u>reducing said reference voltage...[when] said digital signal...[has changed to be] less than said reference voltage.</u> Claim 10 calls for <u>increasing said reference voltage...[when] said digital signal...[has changed to be] greater than said reference voltage.</u> Claim 12 calls for <u>comparing...to said first nominal reference level when said signal is closer to said first nominal reference level than said second nominal reference level</u> (and visa versa). As evident from the discussion, above, the switching action described in Lippmann compares the signal to the reference voltage that is

farthest from the input signal. Claims 14-17 call for the voltage difference between said electrical [high or low, depending upon the claim] level and said reference voltage ...[to be] decreased.... Claim 18 calls for moving a reference voltage...[to] a second voltage level that is closer to [the] received voltage level. Finally, applicant's claim 19 calls for signal control...[that] adjusts said reference signal to approach said input signal. The actions called for in applicant's above mentioned independent claims all call for an action by or on the reference signal that is the opposite of that disclosed in Lippmann. Therefore, Lippmann does not teach, disclose, or suggest all of the limitations of applicant's independent claims.

"A claim is anticipated only if each and every element as set forth in the claims is found ... in a single prior art reference" *Verdegall Bros. v. Union Oil co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Accordingly, since Lippmann discloses an action that is the opposite of what applicant is claiming, applicant's independent claims are not anticipated by Lippmann.

Furthermore, applicant's invention is not obvious in view of Lippmann. "To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974)" MPEP 2143.03. Since Lippmann discloses an action that is the opposite of what applicant is claiming, Lippmann does not teach or suggest all of applicants claim limitations. Accordingly, applicant respectfully submits that applicant's invention is not obvious in view of Lippmann.

8. Claims 2-3, 7, 9, 11, and 22 were rejected under 35 U.S.C. 103(a) as being unpatentable over Lippmann et al. These claims are dependent upon independent claims discussed above. Since, for the reasons discussed above, the applicant's independent claims are not anticipated or obvious in view of Lippmann, applicant's dependent claims are also not anticipated or obvious in view of Lippmann.

9. Carobolante (5,376,834), Beck (6,225,929) and Kuboli (4,527,148) were made of record but not relied upon. These references, either alone or in combination, do not disclose, teach and suggest all of applicant's claim limitations.

10. This application is considered in condition for allowance and such action is earnestly solicited.

Respectfully submitted

by

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Version with Markings to Sh w Changes Made

IN THE SPECIFICATION:

The title has been amended as follows:

DYNAMIC CONTROL OF SWITCHING REFERENCE_VOLTAGE

IN THE CLAIMS:

1. (Amended) A method, comprising:

moving a reference voltage from a first voltage level to a second voltage level wherein said second voltage level is closer to a received voltage level than said first voltage level; and,

~~level and wherein~~comparing said reference voltage~~is compared~~ to said received voltage level to determine a digital state of said received voltage level.

2. (Amended) The method of claim 1 wherein said ~~movement~~moving said reference voltage from said first voltage level to said second voltage level takes place over a period of time that is on the order of the one-half the minimum time said received voltage level is expected to remain in one digital state.

3. The method of claim 2 further comprising:

moving said reference voltage from said second voltage level to said first voltage level wherein said first voltage level is closer to said received voltage level than said second voltage level.

4. A method, comprising:

comparing a parameter of an input signal to a parameter of a reference to determine a logical state of said input signal; and,

adjusting said parameter of said reference to reduce a difference between said parameter of said reference and said parameter of said input signal.

5. The method of claim 4 wherein said difference between said parameter of said reference and said parameter of said input signal maintains a nonzero minimum difference.

6. A method, comprising:

comparing a parameter of an input signal to a parameter of a reference to determine a logical state of said input signal wherein said parameter of said input signal has a nominal value representing a logical low and a nominal value representing a logical high; and,

adjusting said parameter of said reference to reduce a difference between said parameter of said reference and said parameter of said input signal and said parameter of said reference signal stays between said nominal value representing said logical low and said nominal value representing said logical high.

7. The method of claim 6 wherein said parameter of said reference is adjusted over a period of time that greater than 0.25 and less than 1.5 times the minimum expected period of time that said input signal will remain in a single logical state.

8. A method of receiving a digital signal, comprising:

comparing said digital signal to a reference voltage;

determining when said digital signal has changed from being greater than said reference voltage to being less than said reference voltage; and,

reducing said reference voltage after said digital signal has changed from being greater than said reference voltage to being less than said reference voltage.

9. The method of claim 8 wherein said reference voltage is reduced over a period of time that is greater than an expected period of time for said digital signal to change from one digital state to another.

10. A method of receiving a digital signal, comprising:

comparing said digital signal to a reference voltage;

determining when said digital signal has changed from being less than said reference voltage to being greater than said reference voltage; and,

increasing said reference voltage after said digital signal has changed from being less than said reference voltage to being greater than said reference voltage.

11. The method of claim 10 wherein said reference voltage is increased over a period of time that is greater than an expected period of time for said digital signal to change from one digital state to another.

12. A method, comprising:

adjusting a reference between a first nominal reference level and a second nominal reference level;

adjusting said reference between said second nominal reference level and saidfirst nominal reference level;

comparing a signal to said first nominal reference level when said signal is closer to said first nominal reference level than said second nominal reference level; and,

comparing said signal to said second nominal reference level when said signal is closer to said second nominal reference level than said first nominal reference level.

13. The method of claim 12 wherein said steps of comparing are used to initiate said steps of adjusting so that said reference becomes closer to said first nominal reference level after said signal has crossed said second nominal reference level and so that said reference becomes closer to said second nominal reference level after said signal has crossed said first nominal reference level.

14. (Amended) A method of controlling a reference voltage, comprising:

tracking an input voltage with said reference voltage such that the voltage difference between an electrical high level of the input voltage and said reference voltage is increased by the change in said input signal as said input signal transitions from an electrical low level to said electrical high level and the voltage difference between said electrical high level and said reference voltage is decreased by increasing said reference voltage after said input signal transitions.

15. (Amended) A method of controlling a reference voltage, comprising:

tracking an input voltage with said reference voltage such that the voltage difference between an electrical low level of the input voltage and said reference voltage is increased by the change in said input signal as said input signal transitions from an electrical high level to said electrical low level and the voltage difference between said electrical low level and said reference voltage is decreased by decreasing said reference voltage after said input signal transitions.

16. (Amended) An apparatus, comprising:

an input voltage;

a reference voltage; and,

means for ~~tracking an input voltage with~~changing said reference voltage to track said input voltage such that the voltage difference between an electrical high level of the input voltage and said reference voltage is increased by the change in said input signal as said input signal transitions from an electrical low level to said electrical high level and the voltage difference between said electrical high level and said reference voltage is decreased by increasing said reference voltage after said input signal transitions.

17. (Amended) An apparatus, comprising:

an input voltage;

a reference voltage; and,

means for ~~tracking an input voltage with~~changing said reference voltage to track said input voltage such that the voltage difference between an electrical low level of the input voltage and said reference voltage is increased by the change in said input signal as said input signal transitions from an electrical high level to said electrical low level and the voltage difference between said electrical low level and said reference voltage is decreased by decreasing said reference voltage after said input signal transitions.

18. (Amended) A circuit, comprising:

a reference voltage;

a received voltage having a received voltage level; and,

means for moving ~~a~~said reference voltage from a first voltage level to a second voltage level wherein said second voltage level is closer to ~~a~~said received voltage level than said first voltage level and wherein said reference voltage is compared to said received voltage level to determine a digital state of said received voltage level.

19. (Amended) A circuit comprising:

a differential receiver that compares an input signal and a reference signal to determine a digital state for said input signal; and,

a reference signal control responsive to said differential receiver that adjusts said reference signal over a period of time to approach said input signal.

20. The circuit of claim 19 wherein said reference signal control comprises:

a saturating counter wherein a count direction of said counter is responsive to said differential receiver; and,

an analog MUX responsive to said saturating counter that selects one of a plurality of input voltages and outputs that one of said plurality of voltages to be used as said reference signal.

21. The circuit of claim 20 wherein said plurality of voltages are generated by a resistive ladder.

22. The circuit of claim 20 wherein said saturating counter is clocked by a clock signal having a period that is much less than the minimum expected time for said input signal to remain in one logical state.